Automatic ESD Tester with Ultra-low Parasitic Inductance & Capacitance

ESD Tester



HED-S5000R series

Conforms to JEDEC, ESDA, JEITA standards

Testing under any world standard is possible

This system's uniquely short discharge circuit is made possible by its original mechanical design. The short circuit minimizes the influence of inductance and capacitance on the data. Further, the use of a single circuit ensures data stability for each device pin tested.

Features

- ◆Single discharging circuit

 New, specialized mechanical GND setting

 Ultra-low parasitic inductance & capacitance
- ♦ Max 256 pins
- ◆Can be used with various standard waveforms

 This high-quality system conforms to a number of international standards, including JEDEC, ESDA, AEC, and JEITA.
- ◆Can be used with latch-up testing
- ◆Easy and reliable operation

 Much shorter testing procedure

Auto-test system



HED-S5000R Outline

<Judgment Methods>

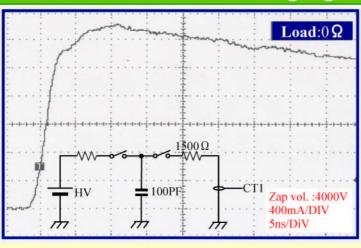
Variable quantity : relative to initial current Absolute quantity : threshold e value

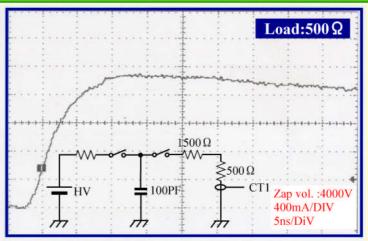
<Current Leak Measurement>

Measurement voltage Vf can be set for up to 20 points per table.

Data can be displayed in a list (volume per Vf/lf) or graph.

Discharging waveform(HBM)



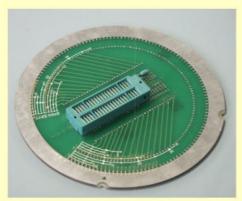


In addition to above discharging waveform, adaptable to Machine Model for JEDEC and ESD Association.

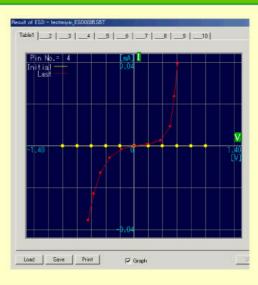
Measurement result screen







Socket board



Specification

Test pins

Built-in capacity/resistor

Pulse voltage

Voltage step

Zap number

Zap interval time

Charging voltage accuracy

Measurement voltage(Vf)

Accuracy of current measurement

Outer dimensions

Weight

Control

AC Voltage

MAX 256 pins

HBM/MM,10PF

+/-10V - +/-8000V

Min.5V

1-99 times (Max 65535)

0.1 - 9.9s

1%+/-10V

+/-40 (Step 0.1V)

1%+/-(1/500FS+/-10nA)

 $545(W) \times 350(D) \times 290(H)$

25Kg

Windows or Stand alone

100 - 240V/5A

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Agency

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